PCIe® 4.0 Electrical Compliance Testing Deep Dive

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Disclaimer

The information in this presentation refers to specifications still in the development process. This presentation reflects the current thinking of various PCI-SIG® workgroups, but all material is subject to change before the specifications are released.

PCIe® 4.0
Electrical Tests Under Development

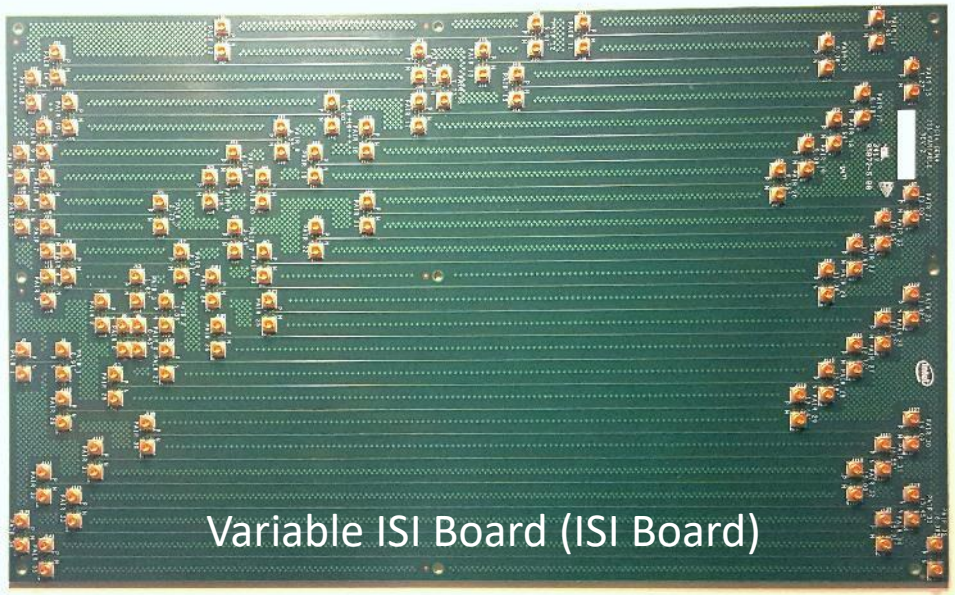
- **Transmitter (Tx) Signal Quality Test at 16GT/s**
  - End of channel eye diagram (eye width & eye height)
- **Tx Preset Equalization Test at 16GT/s**
  - Measures voltage levels for Preset 0 to Preset 10
- **Tx Pulse Width Jitter at 16GT/s (Add-in Card)**
  - Clock pattern used to measure the Base Spec Pulse Width Jitter limit
- **PLL Bandwidth (Add-in Card)**
  - Verifies an Add-in Card's PLL bandwidth & peaking
- **Link Equalization Handshaking at 16GT/s**
  - Tx starts with correct preset requested through protocol
  - Tx responds to protocol changes and adjusts
  - Receiver (Rx) correctly adjusts the link Tx and operates with a stressed eye
- **All 2.5/5.0/8.0GT/s Testing Still Required for 4.0 Integrators List for a 16GT/s Capable Device**

PCIe 4.0 Electrical Test Fixture Characterization

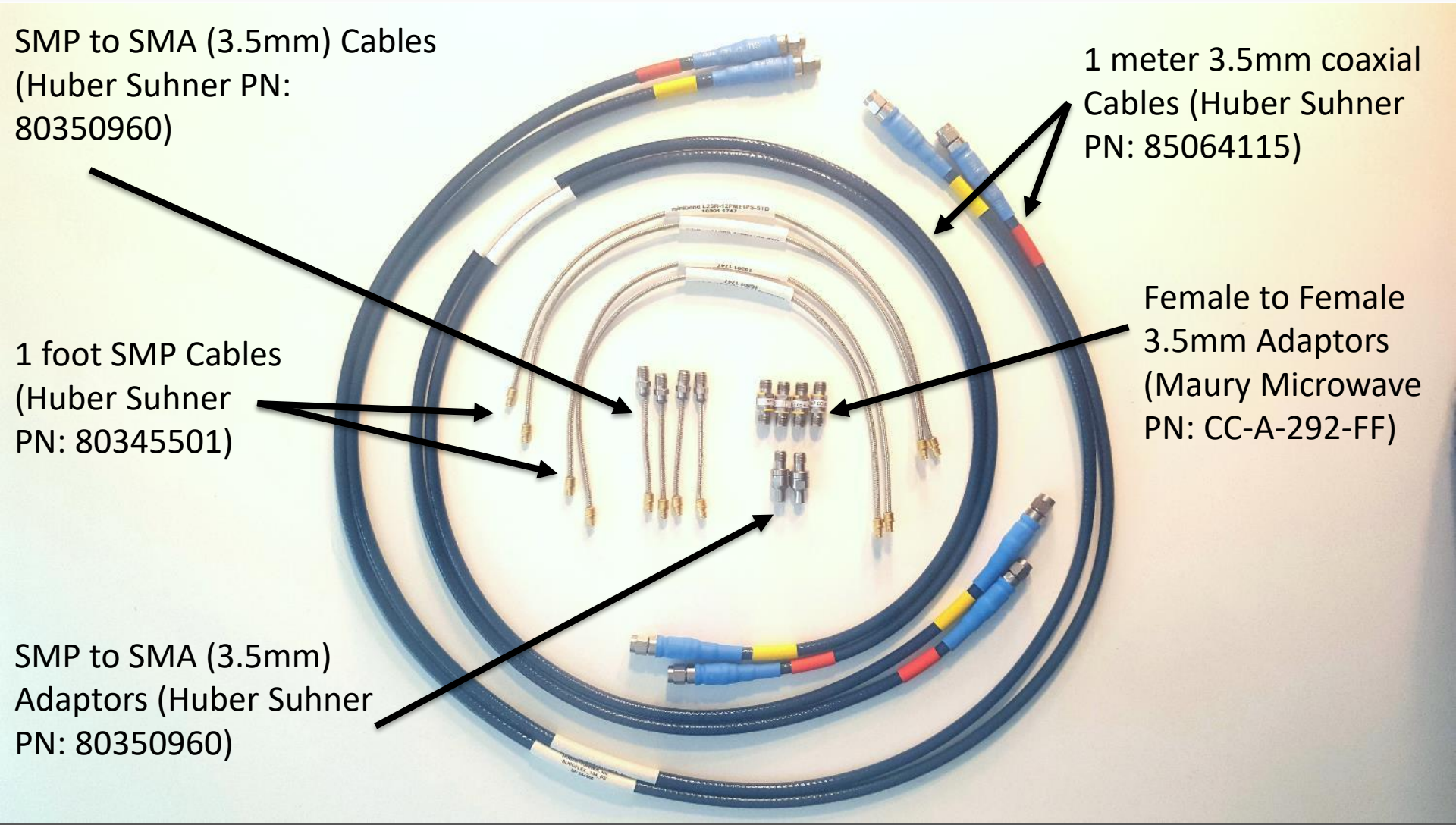
PCIe 4.0
Electrical Test Fixture Characterization

- **Vector Network Analyzer (VNA) Based Test Fixture Characterization**
  - PCIe Tx Signal Quality Test at 16GT/s
  - PCIe Rx Calibration at 16GT/s
  - PCIe Link Equalization Rx Test at 16GT/s
- **Selection of Variable ISI Pairs**
  - VNA measurements are used to select a variable ISI pair(s) which provide the correct amount of differential Insertion Loss (IL) at 8 GHz for each test
  - All measurement referencing an “IL” are assumed to be differential insertion loss (SDD21) at 8 GHz
  - The VNA must have a minimum bandwidth of 20 GHz for this characterization
- **Inclusion of Coaxial Cables & Adaptors**
  - Characterization is performed with coaxial cables & adaptors
  - The variable ISI pair selection will comprehend the loss of coaxial cables and adaptors used in the electrical tests

PCIe 4.0 Fixture Characterization: Test Fixture Boards



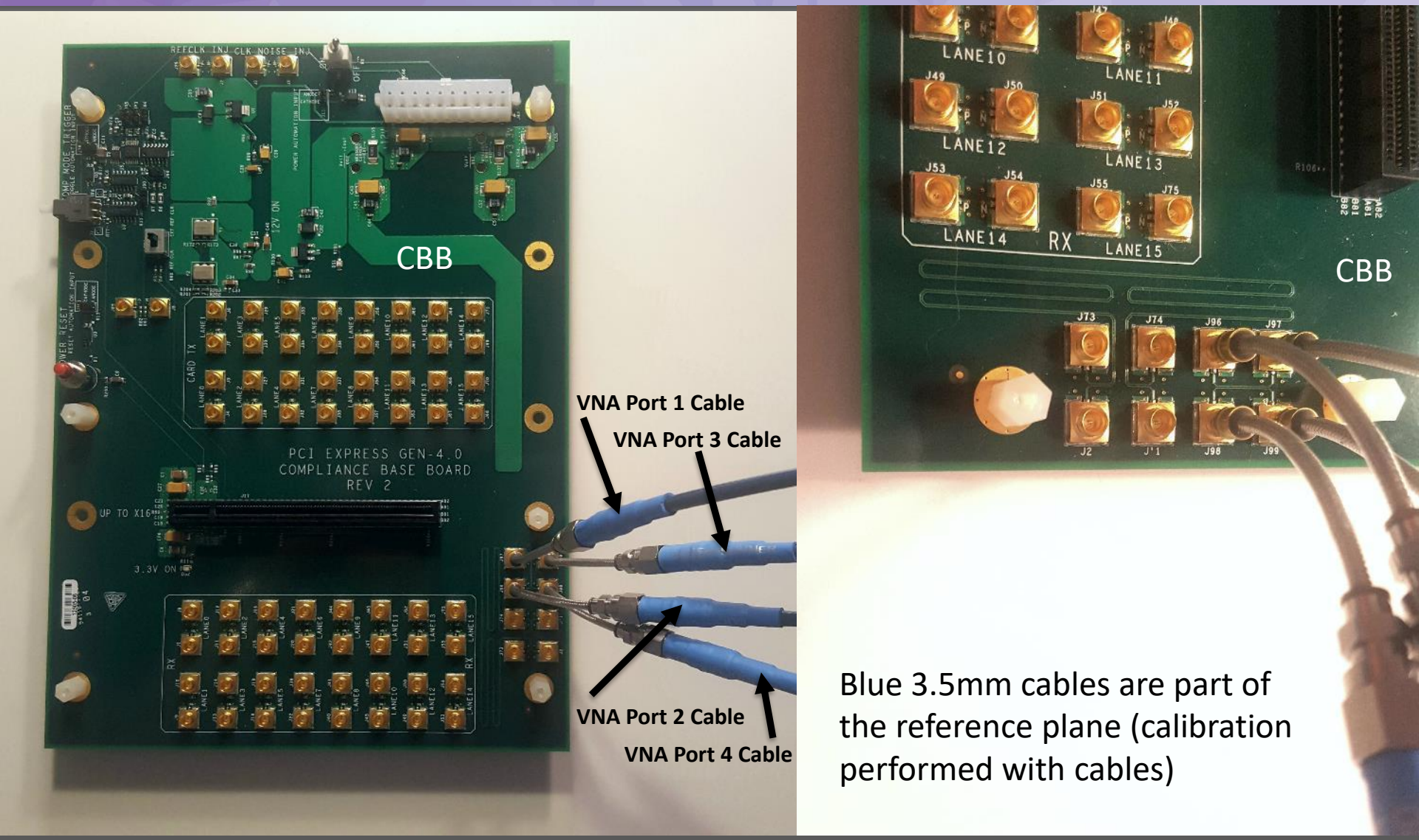
PCIe 4.0 Fixture Characterization: Cables & Adaptors



PCIe 4.0 Fixture Characterization: Insertion Loss per Inch

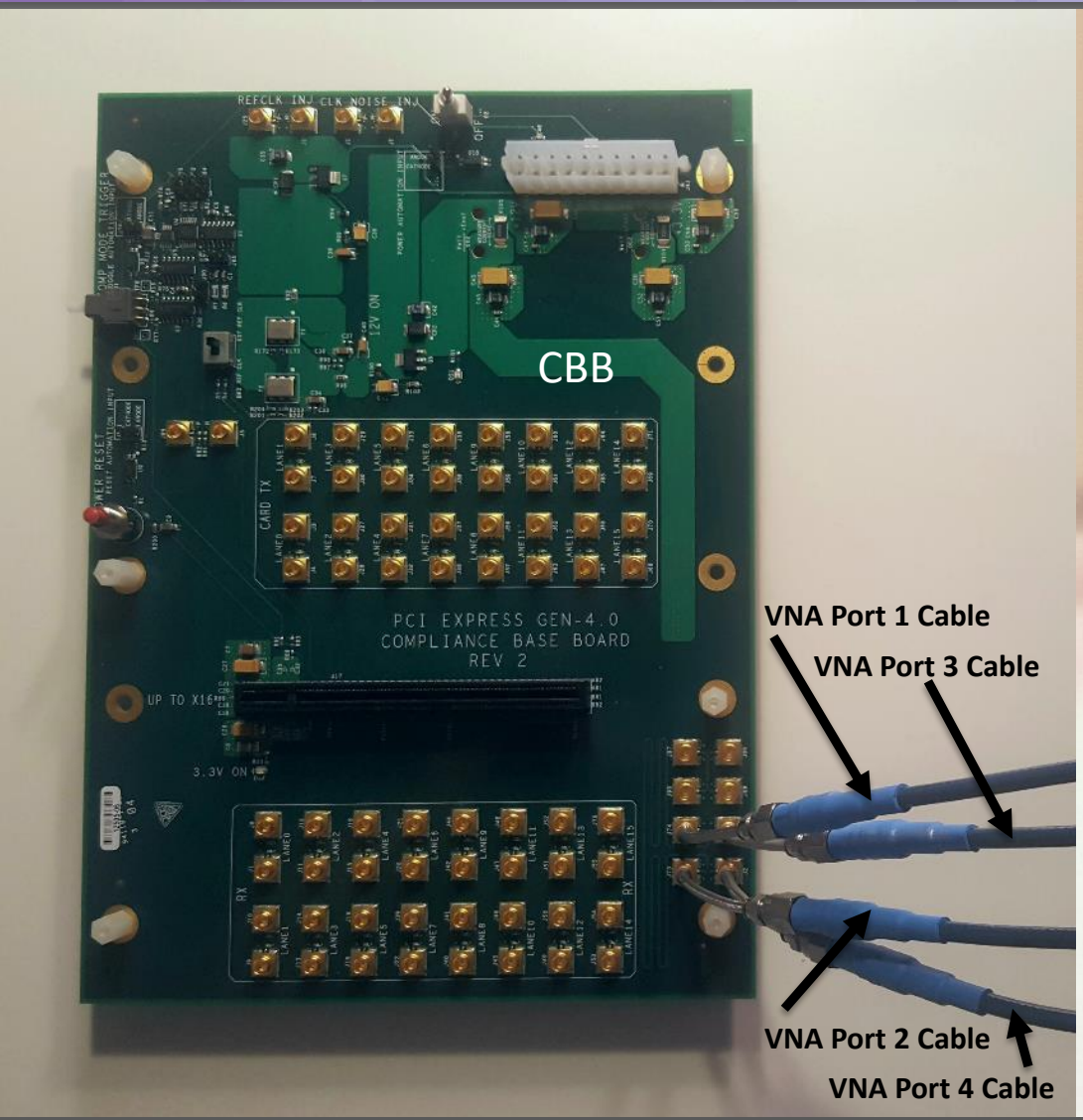
- **Determine Loss per Inch of PCBs**
  - The test fixture insertion IL per inch is necessary to accurately estimate the differential trace IL of the CBB & CLB up to the CEM connector
- **Short & Long Trace Measurements**
  - SMP to SMA cables are included in these measurements
  - Measure IL of the short trace (J97/J99 to J96/J98) on the CBB
  - Measure IL of the long trace (J1/J74 to J2/J73) on the CBB
    - The difference in length between the long trace and short trace is 10 inches
  - IL/Inch = (IL long Trace – IL Short Trace) / 10

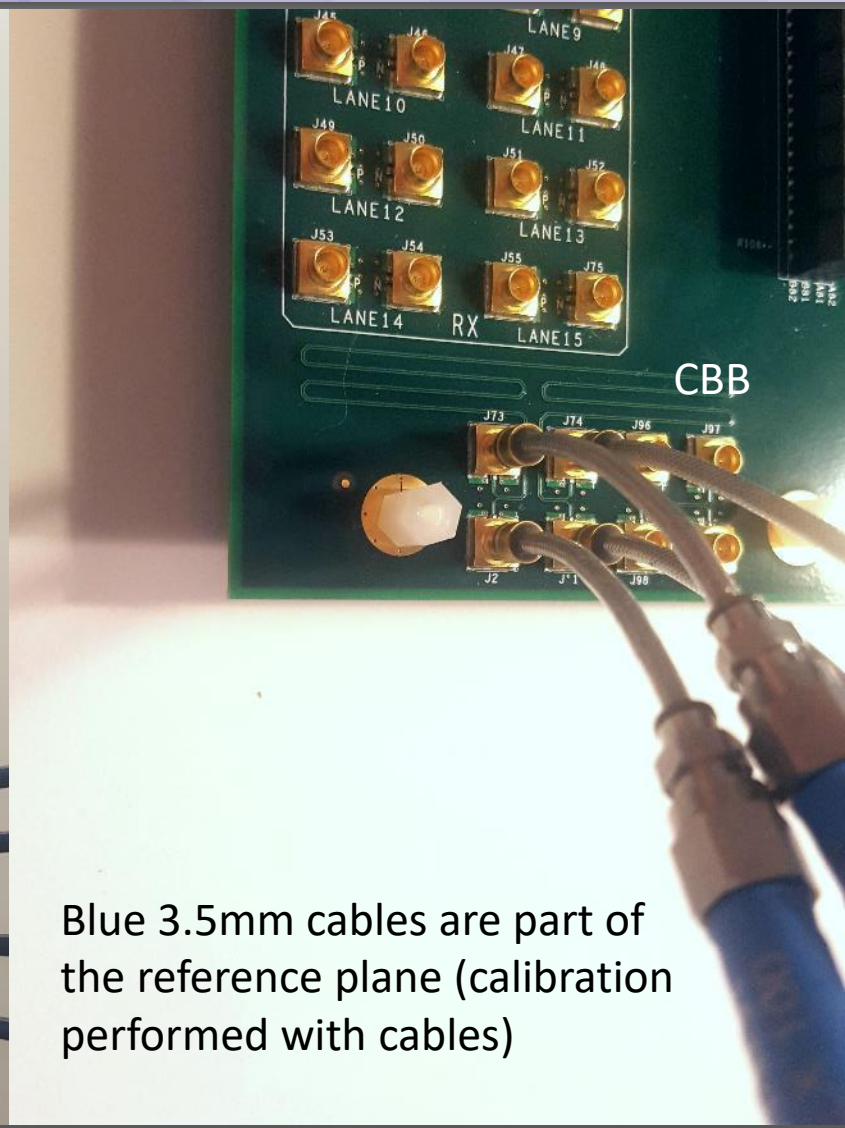
PCIe 4.0 Fixture Characterization: Insertion Loss per Inch (Short Trace)



Blue 3.5mm cables are part of the reference plane (calibration performed with cables)

PCIe 4.0 Fixture Characterization: Insertion Loss per Inch (Long Trace)





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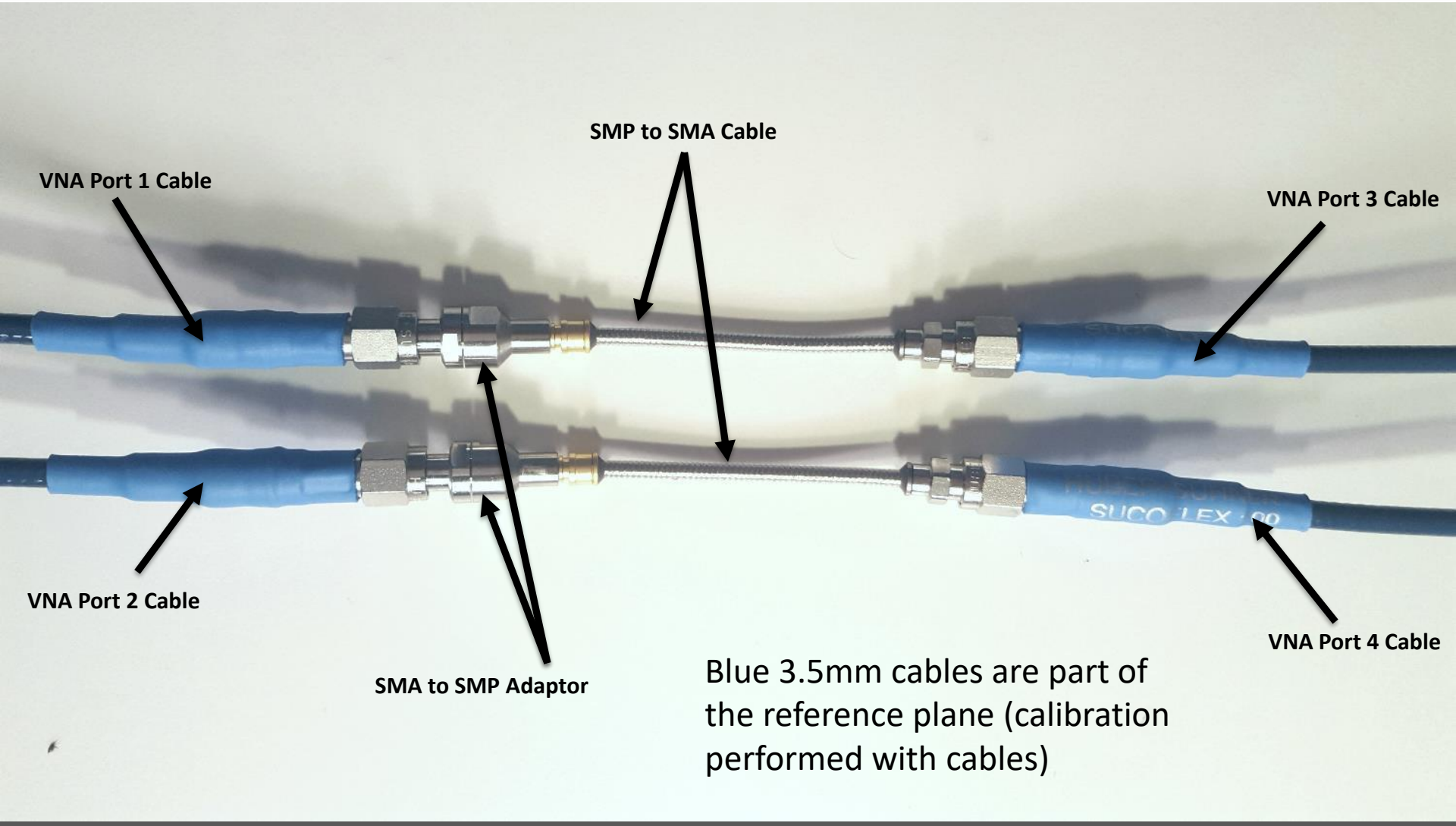
PCIe 4.0 Fixture Characterization: Coaxial Launch Loss

- **Determine Loss of SMP to SMA Cable**
  - SMP to SMA adaptor IL must be comprehended for removal
  - If Huber Suhner adaptors (PN: 80350960) are used an IL of 0.2225 dB may be assumed
  - If different adaptors are used the IL must be measured
    - One possible measurement technique
      - SMA to SMP Adaptor <-> SMP to SMA Cable
      - If the IL of the SMA to SMP Adaptor is know this may be removed
- **Coaxial Launch Loss**
  - The Coaxial Launch IL is obtained from the Long Trace IL by removing the IL of the 10 inch trace and the 2 SMP to SMA cables
  - Coaxial Launch IL = (IL long Trace – (10 * IL/Inch) – (2 * IL SMP-SMA Cable)) / 2

PCIe 4.0 Fixture Characterization: Characterize SMP to SMA Adaptor



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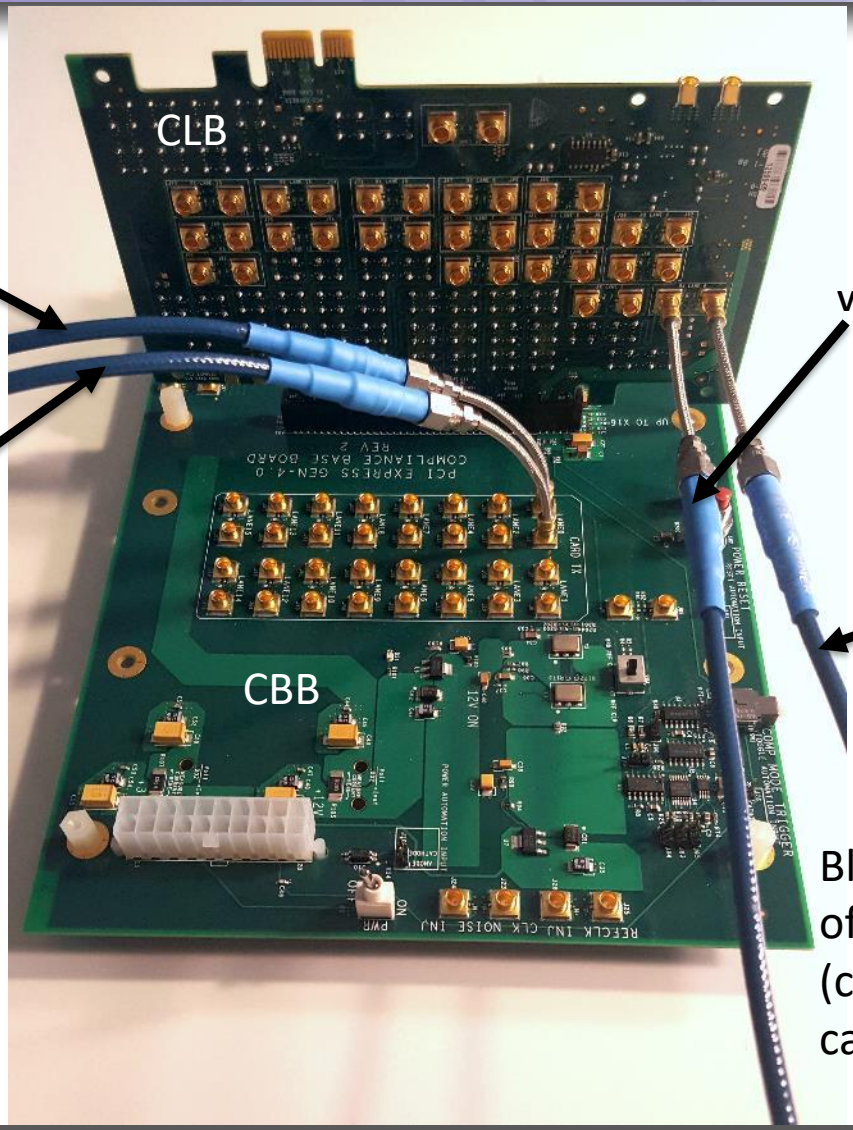
PCIe 4.0 Fixture Characterization: Measure CBB/CLB Loss

- **Determine Loss of CBB & CLB**
  - Measuring the IL of the CLB mated with the CBB establishes an easily measurable loss inclusive of the mated CEM connector
  - The mated CEM connector can then be obtained by removing the IL of cables, coaxial launches, and traces
  - Connect SMP to SMA cables to the CBB Tx Lane 0 and to the CLB Rx Lane 0
  - Plug the CLB (x16) into the CBB and measure IL

PCIe 4.0 Fixture Characterization: Measure CBB/CLB Loss (image)



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PCIe 4.0 Fixture Characterization: Mated CEM Connector Loss

- **Determine Loss of Mated CEM Connector**
  - The Mated CEM Connector (edge fingers of CLB plugged into CEM connector) is needed to determine the IL on each side of the test fixture channels
  - The mated CEM connector loss is obtained by removing the IL of cables, coaxial launches, and traces from the CBB/CLB Loss
  - Mated CEM IL = CBB/CLB IL – (2 * SMP-SMA Cable) - IL/Inch * (CBB Trace Length + CLB Trace Length) – (2 * Coaxial Launch IL)
    - CBB Trace Length = 3”
    - CLB Trace Length = 4”

PCIe 4.0 Fixture Characterization: Determine Loss Split for CBB & CLB

- **Determine Loss of CBB (Including Mated CEM Connector Loss)**
  - The mated CEM connector IL is part of a systems IL budget, so this is included on the CBB side
  - CBB IL = Mated CEM IL+ (IL/Inch * CBB Trace Length) + (2 * Coaxial Launch IL)
    - CBB Trace Length = 3”
- **Determine Loss of CLB (Excluding Mated CEM Connector Loss)**
  - CLB Loss = (IL/Inch * CLB Trace Length) + (2 * Coaxial Launch IL)
    - CLB Trace Length = 4”

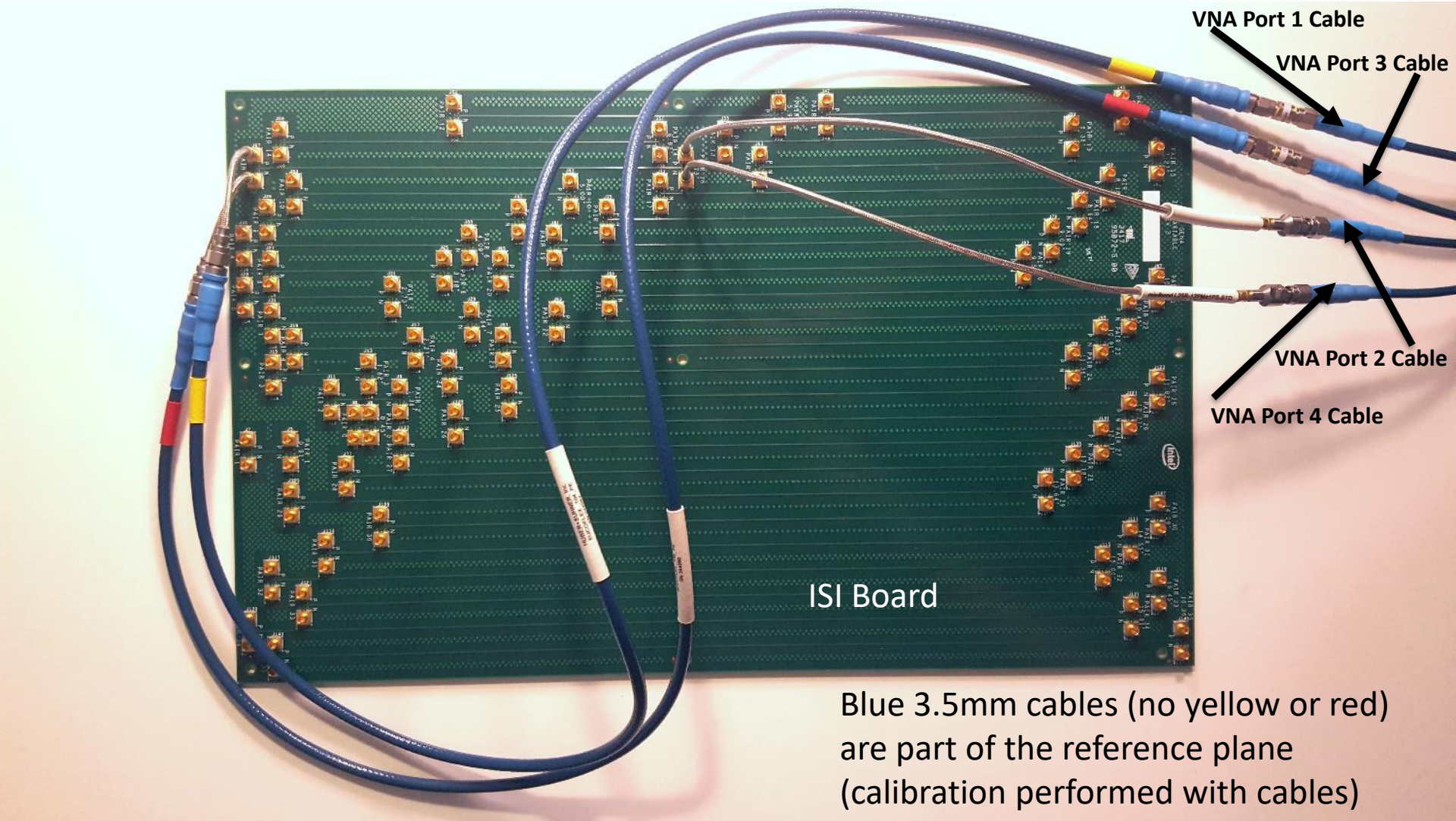
PCIe 4.0 Fixture Characterization: Finding Correct Variable ISI Pairs

- **Target Loss for Each Test Configuration are Determined Based on the CBB & CLB Loss**
- **VNA Measurements are Taken to Find the Variable ISI Pair Matching the Target Loss**
  - Two measurement setups
    - Variable ISI with Cables (Tx Test & DUT side during Rx Calibration)
    - Full Calibration Channel (Rx Calibration – 27/28/30 dB Channels)
      - All cables included
  - If the measurement is less than the target loss, the variable ISI pair is increased
  - If the measurement is more than the target loss, the variable ISI pair is decreased
  - Nominally there should be 0.5 dB steps between ISI pairs

PCIe 4.0 Fixture Characterization: Target Loss Values – System Rx

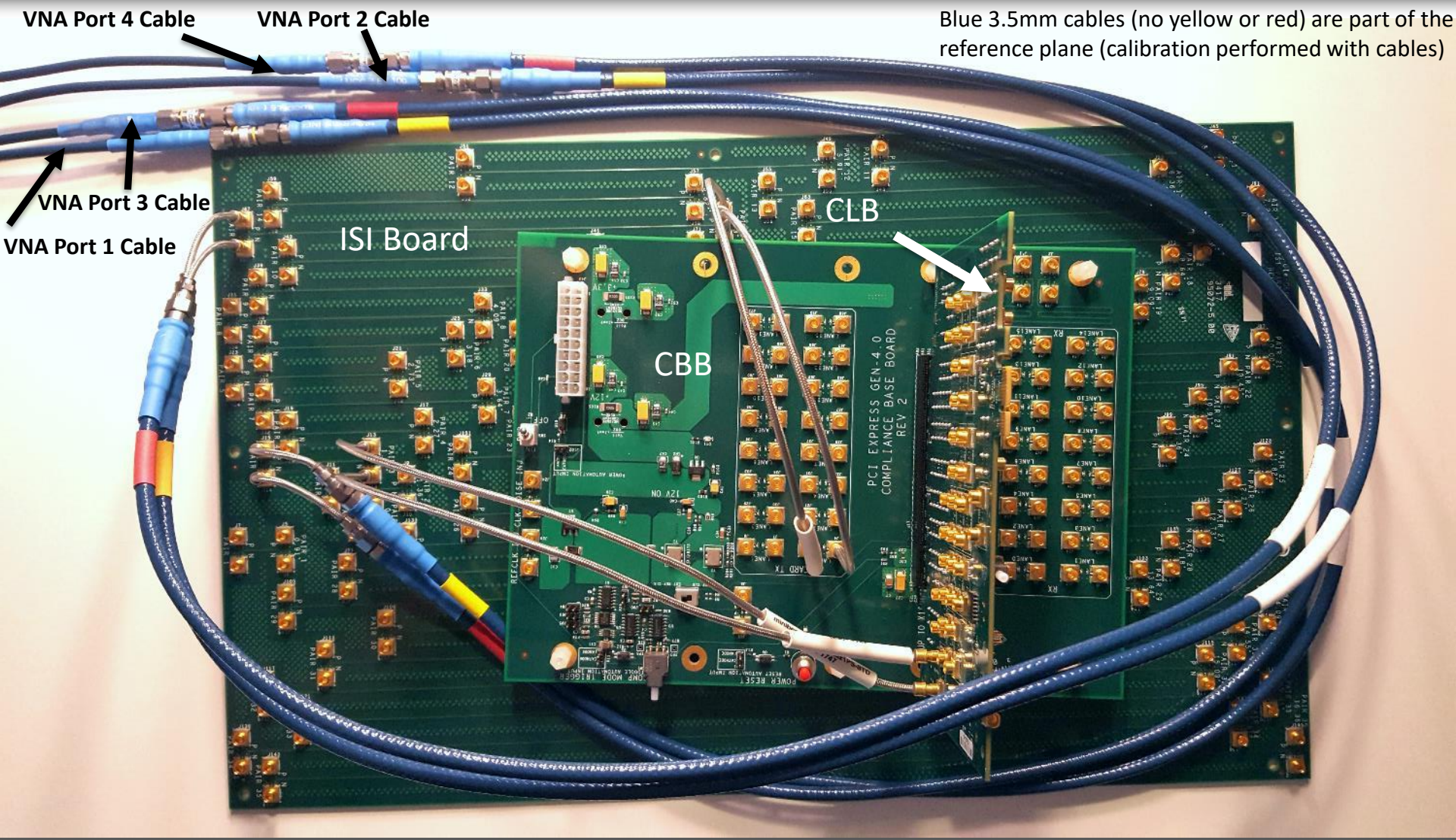
- **Determine Target Loss for System Rx and Find Correct Variable ISI Pair**
  - Variable ISI with Cables (ISI board, SMP cable, & SMA cable)
    - System Rx Calibration CBB Side (20dB fixed)
      - Target Loss = 20dB – 5dB (package embedding) – CBB Loss
      - Measurement Setup
        - SMP Cable <-> Variable ISI Pair X <-> SMA Cable
  - Full Calibration Channel
    - System Rx Calibration CLB ISI (Low – 27dB)
      - Target Loss = 27dB – 5dB (package embedding)
    - System Rx Calibration CLB ISI (Nominal – 28dB)
      - Target Loss = 28dB – 5dB (package embedding)
    - System Rx Calibration CLB ISI (High – 30dB)
      - Target Loss = 30dB – 5dB (package embedding)

PCIe 4.0 ISI Characterization: System Rx CAL (Variable ISI with Cables)



Blue 3.5mm cables (no yellow or red) are part of the reference plane (calibration performed with cables)

PCIe 4.0 ISI Characterization: System Rx CAL (Full Calibration Channel)



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PCIe 4.0 Fixture Characterization: Target Loss Values – Add-in Card Rx

- **Determine Target Loss for Add-in Card Rx and Find Correct Variable ISI Pair**
  - Variable ISI with Cables (ISI board, SMP cable, & SMA cable)
    - Add-in Card Rx Calibration CLB Side (8dB fixed)
      - Target Loss = 8dB – 3dB (package embedding) – CLB Loss
      - Measurement Setup
        - SMP Cable <-> Variable ISI Pair X <-> SMA Cable
  - Full Calibration Channel
    - Add-in Card Rx Calibration CBB ISI (Low – 27dB)
      - Target Loss = 27dB – 3dB (package embedding)
    - Add-in Card Rx Calibration CBB ISI (Nominal – 28dB)
      - Target Loss = 28dB – 3B (package embedding)
    - Add-in Card Rx Calibration CBB ISI (High – 30dB)
      - Target Loss = 30dB – 3dB (package embedding)

PCIe 4.0 ISI Characterization: AIC Rx CAL (Variable ISI with Cables)

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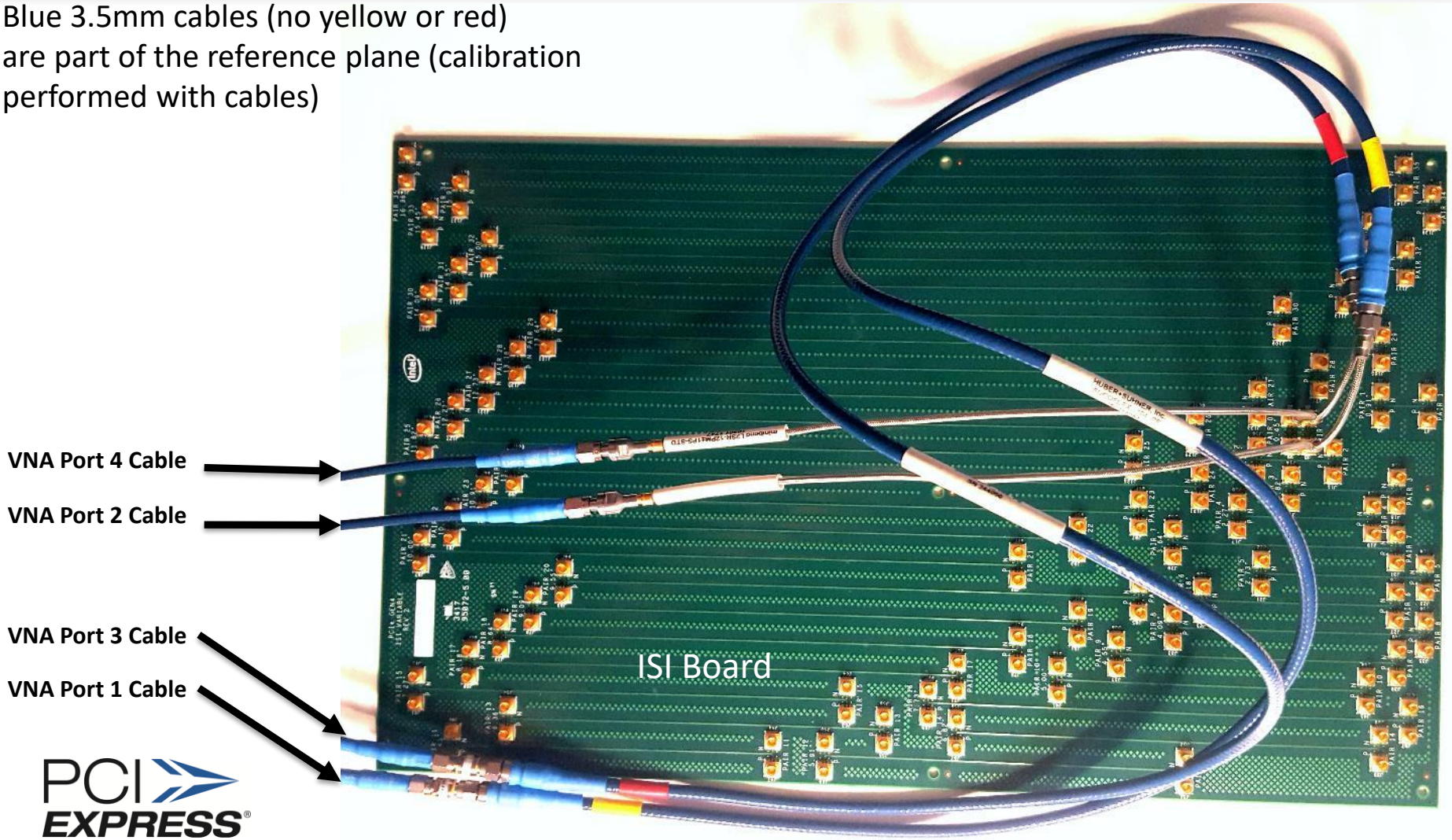
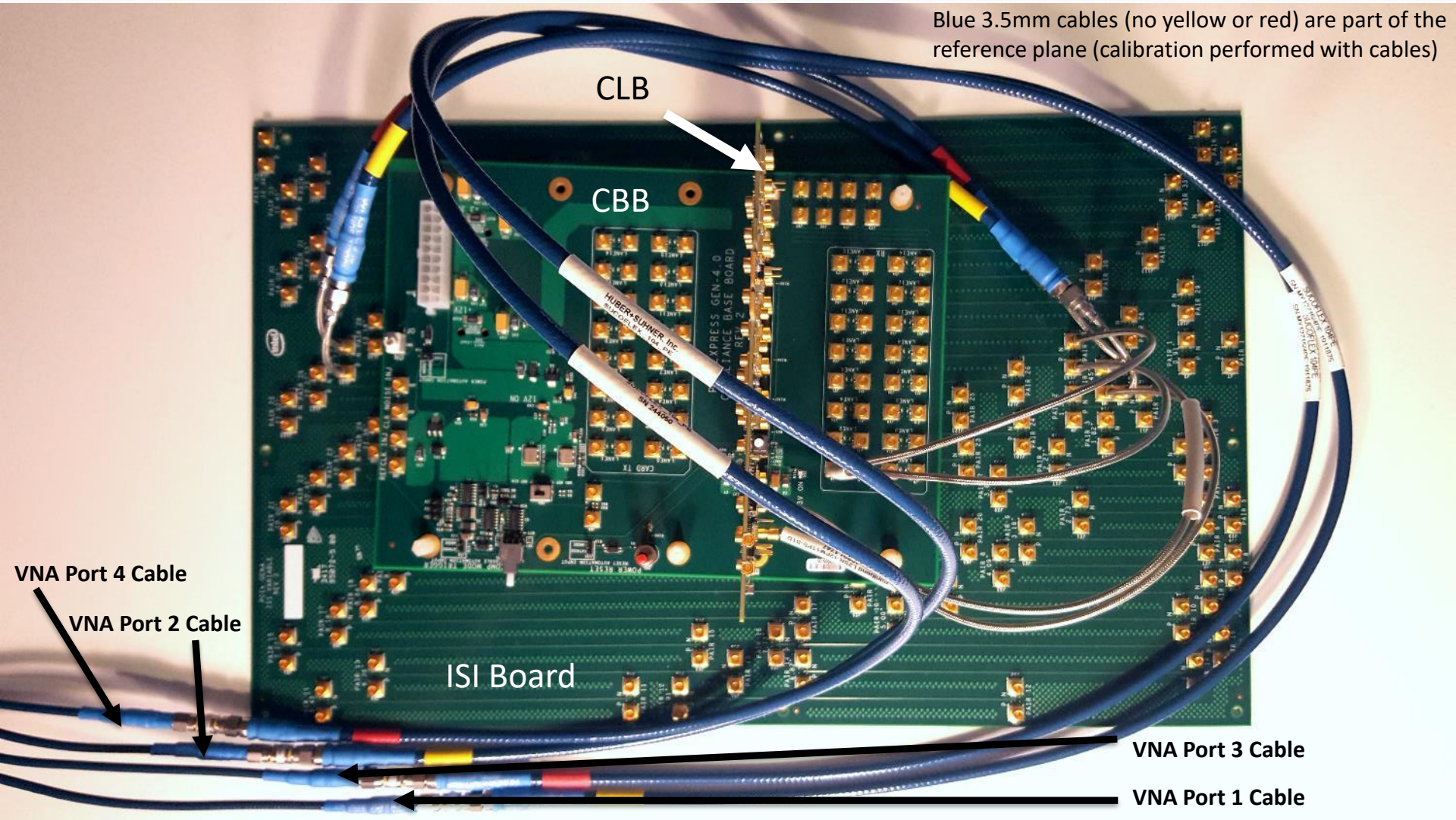


PCIe 4.0 ISI Characterization: AIC Rx CAL (Full Calibration Channel)



PCIe 4.0 Fixture Characterization: Target Loss Values – Tx Signal Quality

- **Determine Target Loss for Add-in Card Rx and Find Correct Variable ISI Pair**
  - Variable ISI with Cables (ISI board, SMP cable, & SMA cable)
    - System Tx Signal Quality Test
      - Target Loss = 8dB – 3dB (package embedding – CLB Loss
      - Measurement Setup
        - SMP Cable <-> Variable ISI Pair X <-> SMA Cable
    - Add-in Card Tx Signal Quality Test
      - Target Loss = 20dB – 5dB (package embedding) – CBB Loss

PCIe 4.0 ISI Characterization: AIC Tx (Variable ISI with Cables)

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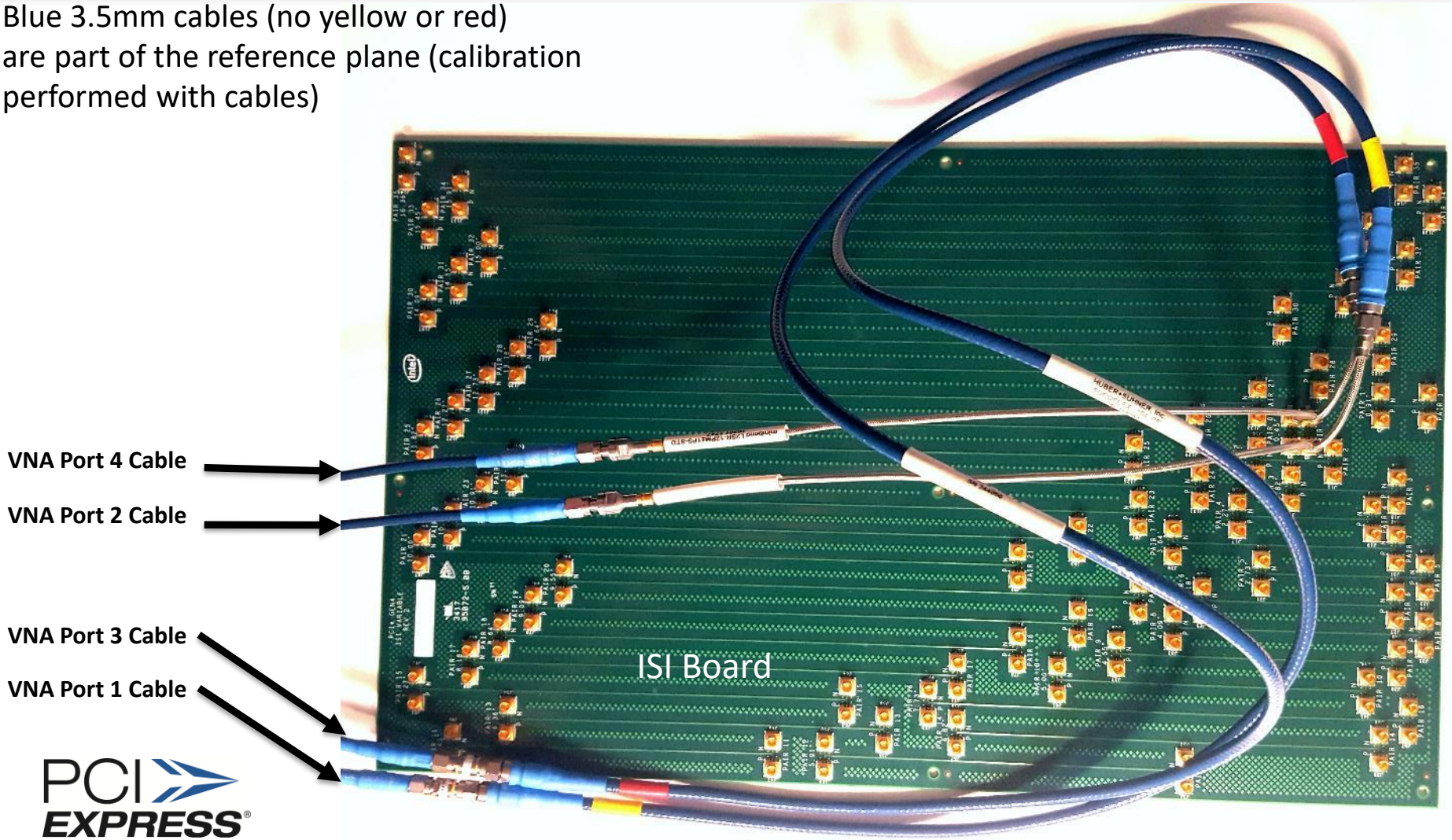
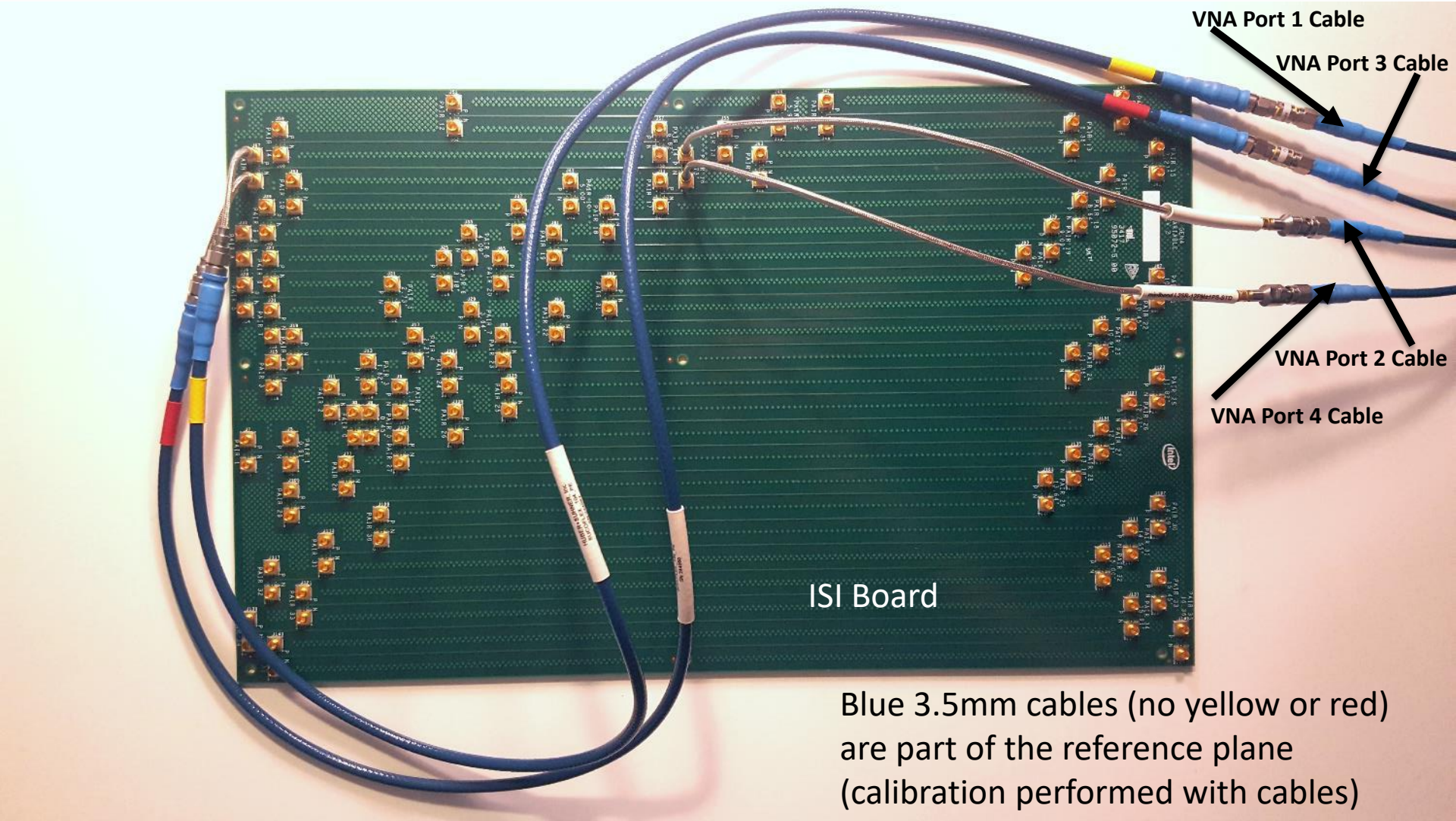


PCIe 4.0 ISI Characterization: System Tx (Variable ISI with Cables)



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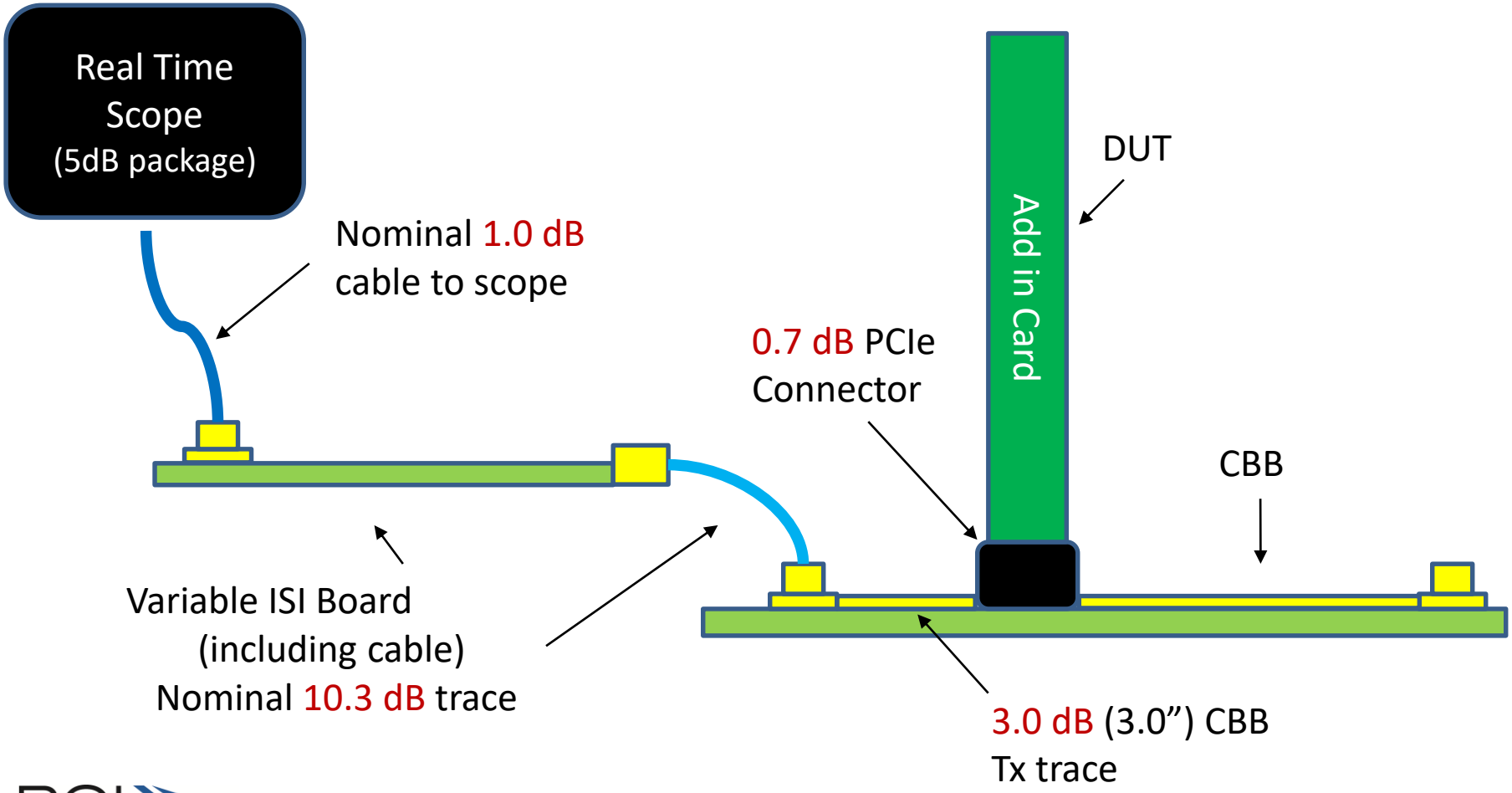
PCIe 4.0 Electrical Tests

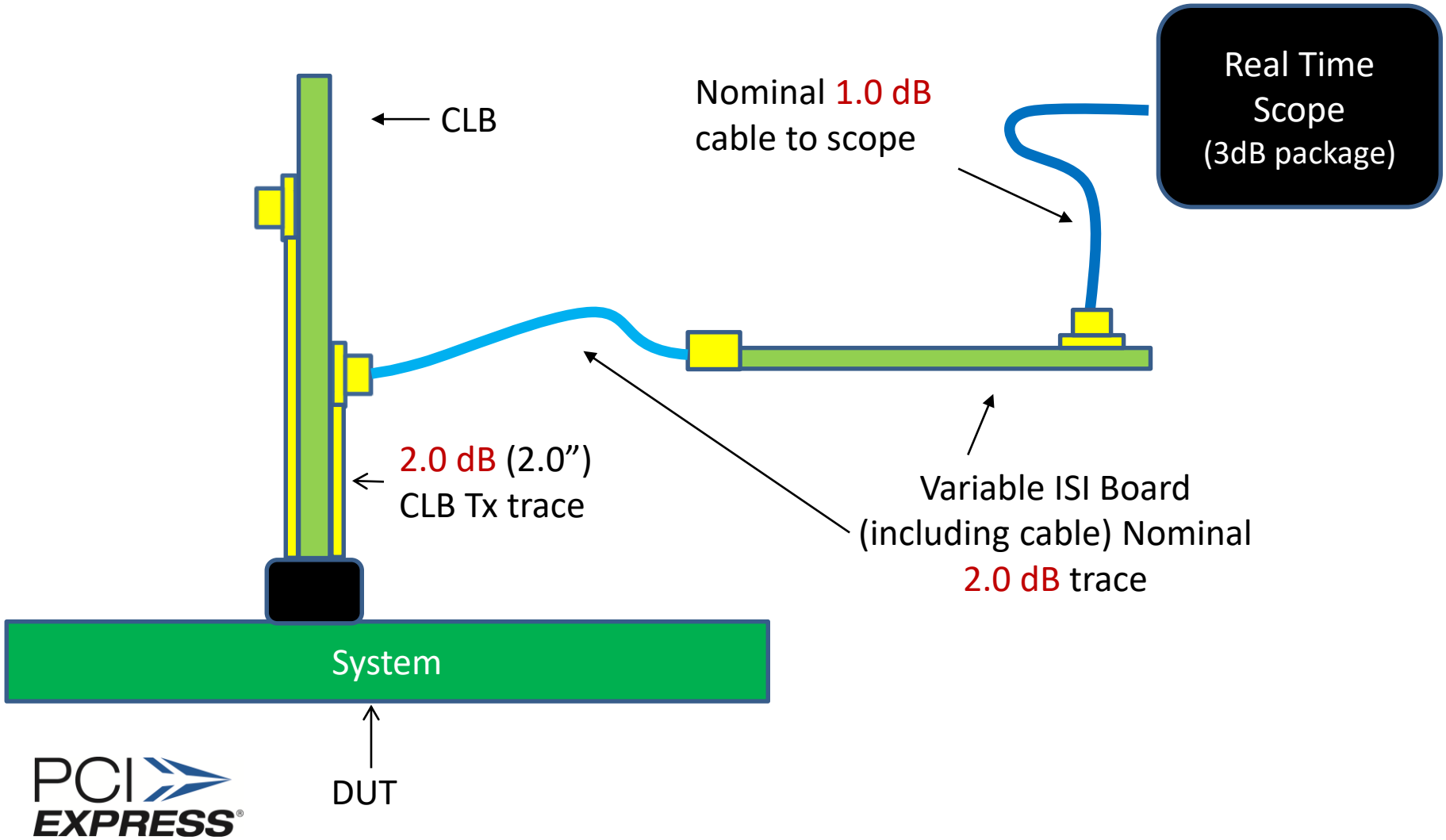
PCIe 4.0 (Add-in Card)
Tx Signal Quality Test at 16GT/s



PCIe 4.0 (Add-in Card)
Tx Signal Quality Test at 16GT/s

- **Channel Setup**
  - Add-in Card plugs into CBB -> Variable ISI Board -> Scope
  - 20dB at 8GHz of additional loss (including package embedding)
- **Power on CBB**
- **Scope bandwidth is 25GHz**
- **5dB package model embedded on scope**
- **Toggle DUT to transmit 16GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Capture 2.0M UI waveform for every Tx EQ Preset**
- **Waveforms post processed using SigTest**
  - Time Domain CDR algorithm used to recover clock
  - Behavioral Rx Equalization applied
  - Eye width & Eye height @ E-12
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
    - EW > 24.75 ps
    - EH > 23 mV

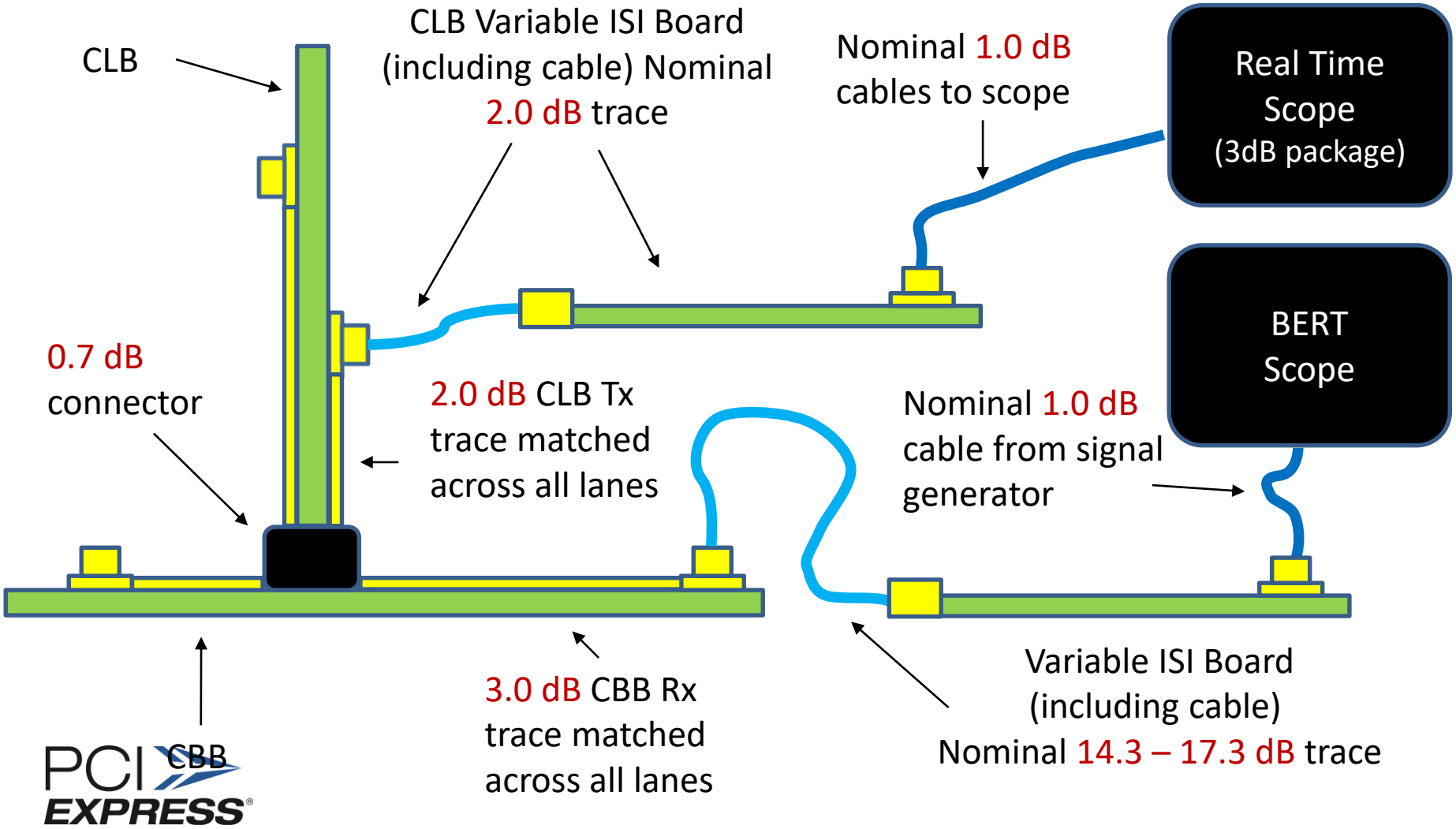
PCIe 4.0 (Add-in Card)
Tx Signal Quality Test at 16GT/s



PCIe 4.0 (System)
Tx Signal Quality Test at 16GT/s

- **Channel Setup**
  - CLB plugs into system -> Variable ISI Board -> Scope
  - 8dB at 8GHz of additional loss (including package embedding)
- **Power on System**
- **Scope bandwidth = 25GHz**
- **3dB package model embedded on scope**
- **Toggle DUT to transmit 16GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Capture 2.0M UI waveform for every Tx EQ Preset**
- **Waveforms post processed using SigTest**
  - Ref clock captured with data waveform and used for clock recovery
  - Behavioral Rx Equalization applied
  - Eye width & Eye height @ E-12
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
    - EW > 21.75 ps
    - EH > 19 mV

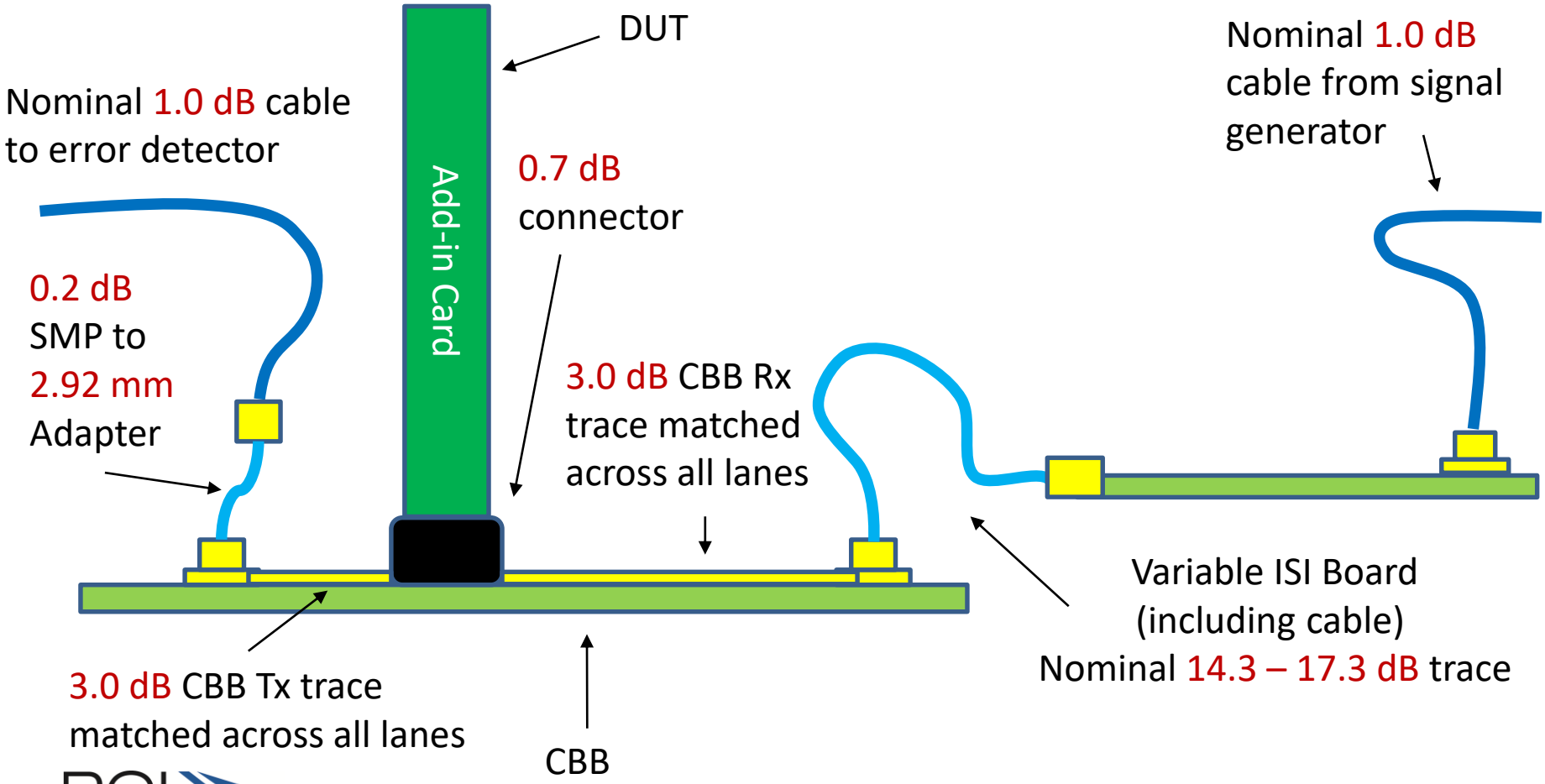
PCIe 4.0 (Add-in Card)
Rx Stressed Eye Calibration at 16GT/s



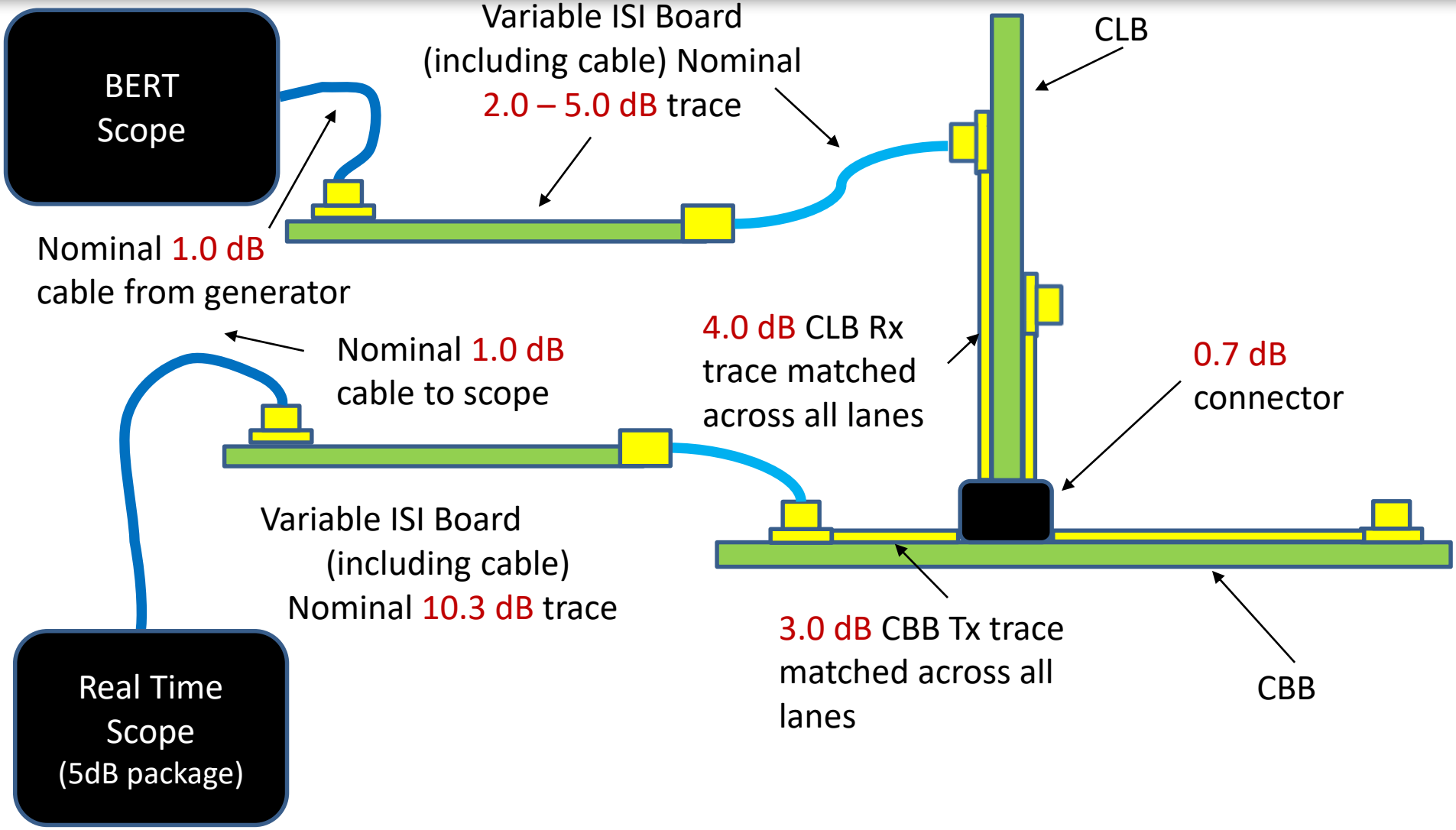
PCIe 4.0 (Add-in Card)
Rx Stressed Eye Calibration at 16GT/s

- **Calibrate Swing & Tx EQ Presets**
  - Setup - SMA cable from BERT to Scope
  - Swing calibrated to 800mV differential
  - Calibrate voltage levels for Preset 0 - 9
- **Calibrate Rj & Sj**
  - Setup - SMA cable from BERT to Scope
  - Rj – 1ps RMS (clock pattern used)
  - Sj – 0.1UI (16GT/s compliance pattern used)
- **Channel Setup**
  - BERT -> Variable ISI -> CBB -> CLB -> Variable ISI -> Scope
  - 27 – 30dB at 8GHz of additional loss (including 3dB package embedding)
- **Calibrate DMI & CMI**
  - DMI – 14mV (End of 27dB Channel)
  - CMI – 150mV (End of 27dB Channel)
- **Channel Selection**
  - Increase channel loss from 27 to 30dB
  - Find channel where the eye width/height is closest to target without dropping below
    - Must use Optimal Tx EQ Preset which is the Preset which gives the largest eye area
- **Eye Width & Eye Height Calibration**
  - Optimal Tx EQ Preset is used with final channel
  - Adjust Sj (5-10ps), DMI (10-25mV), & Swing (720-800mV) until eye width/height (measured with SigTest) targets are achieved
  - EW = 18.75 +/- 0.5ps EH = 15mV +/-1.5mV

PCIe 4.0 (Add-in Card)
Rx Stressed Eye Test at 16GT/s



PCIe 4.0 (System)
Rx Stressed Eye Calibration at 16GT/s



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Rx Stressed Eye Calibration at 16GT/s

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- **Channel Setup**
  - BERT -> Variable ISI -> CLB -> CBB -> Variable ISI -> Scope
  - 27 – 30dB at 8GHz of additional loss (including 5dB package embedding)
- **Calibrate DMI & CMI**
  - DMI – 14mV (End of 27dB Channel)
  - CMI – 150mV (End of 27dB Channel)
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PCIe 4.0 (System)
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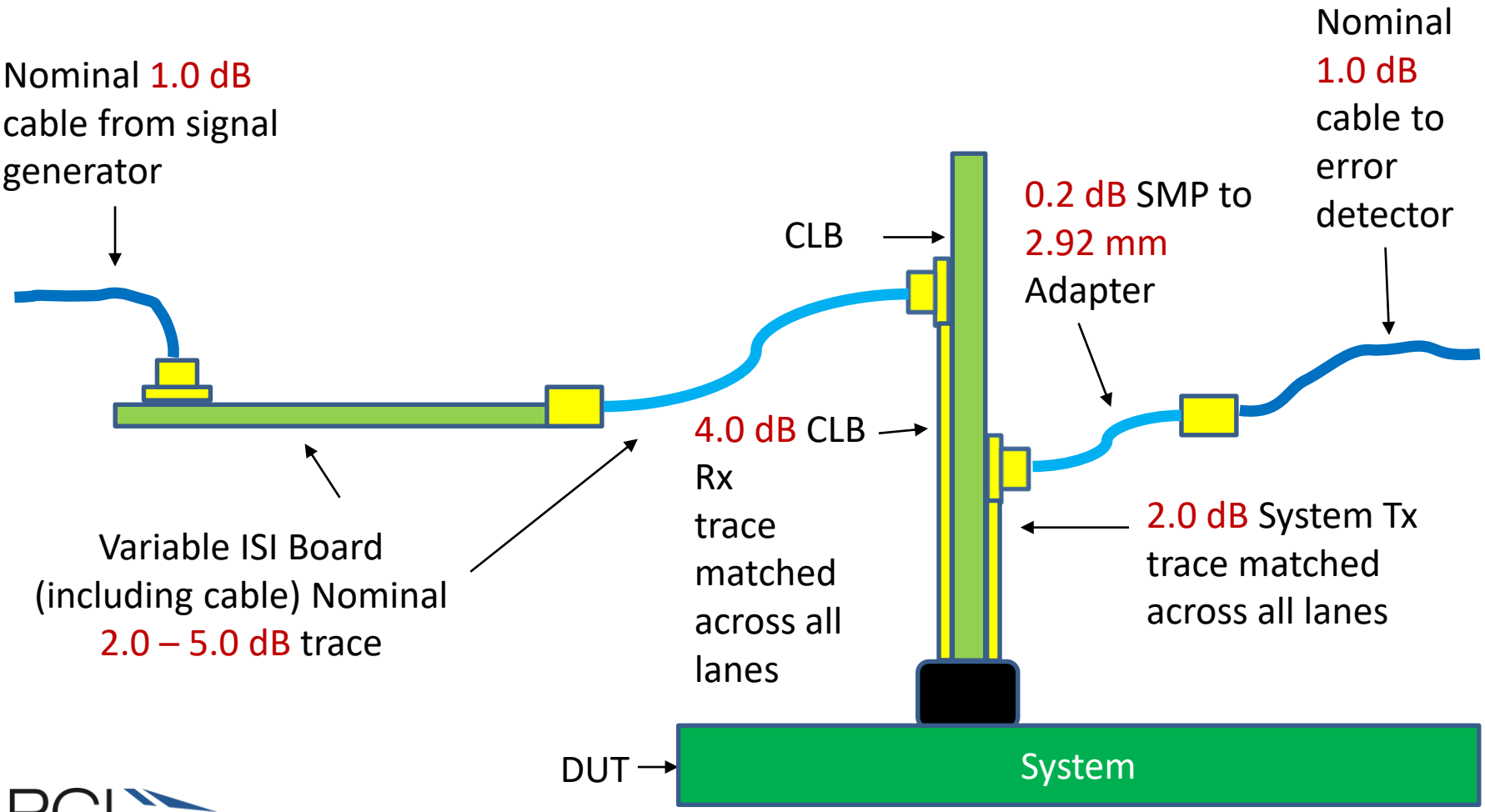

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